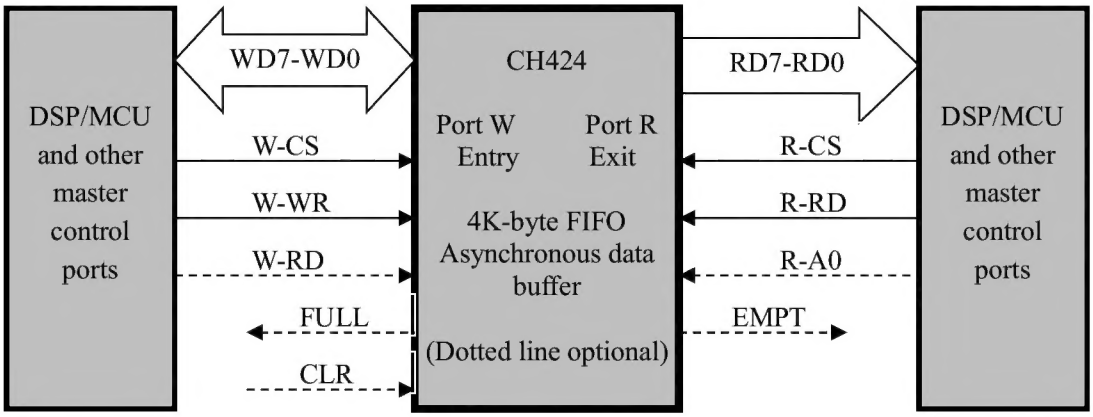
FIFO Memory Chip CH424

Datasheet
Version: 1A
http://wch.cn

1. Overview

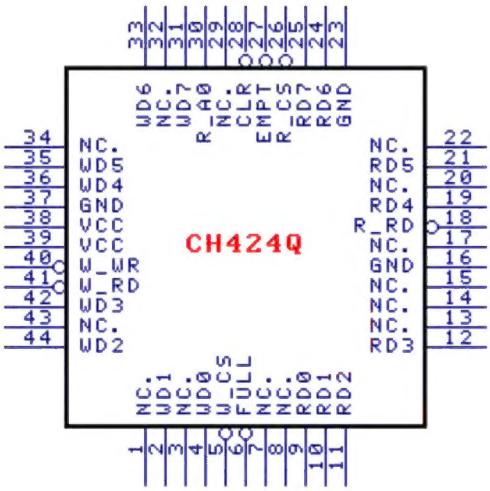
CH424 is a FIFO memory chip with capacity of 4, 000 bytes. CH424 has two 8-bit passive parallel ports: input port W and output port R. CH424 is hooked to the system bus of DSP/MCU/MPU and other controllers through 8-bit data lines as well as read, write and chip selection control lines. It is suitable for connecting MCU to MCU, MCU to DSP/MCU, etc. The figure below shows its general application block diagram.



2. Features

- 4K x 8-bit FIFO.
- 8-bit parallel interface:
  Port W/entry: 8-bit bidirectional three-state data bus (WD7-WD0), chip selection (W_CS), write (W_WR), read (W_RD);
  Port R/exit: 8-bit three-state data bus (RD7-RD0), chip selection (R_CS), read (R_RD), address (R_A0).
- Query the number of bytes of FIFO used space and free space at any time, being easy to read and write in blocks.
- Provide FIFO full state line FULL and FIFO empty state line EMPT, active at low level.
- Support supply voltages of 5V, 3.3V and 3V.
- Adopt QFP-44 lead-free package, and be compatible with RoHS.

3. Package



Package	Width of Plastic		Pitch of Pin		Instruction of Package	Ordering Information
QFP-44	10*10mm		0.8mm	31.5mil	Standard QFP 44-pin patch	CH424Q

4. Pins

Pin No.	Pin Name	Pin Type	Description
38, 39	VCC	Power	Positive power input, an external 0.1uF power decoupling capacitor is required.
16, 23, 37	GND	Power	Common ground
4, 2, 44, 42, 36, 35, 33, 31	WD0～WD7	Bi-directional Three-state	8-bit bidirectional data bus on port W, built-in weak pull-up resistor
5	W_CS	Input	Chip selection control input on port W, built-in weak pull-up resistor, active low
40	W_WR	Input	Write strobe input on port W, built-in weak pull-up resistor, active low
41	W_RD	Input	Read strobe input, built-in weak pull-up resistor, active low
9, 10, 11, 12, 19, 21, 24, 25	RD0～RD7	Three-state output	8-bit data bus on port R
26	R_CS	Input	Chip selection control input on port R, built-in weak pull-up resistor, active low
18	R_RD	Input	Read strobe input, built-in weak pull-up resistor, active low
30	R_A0	Input	Address input on port W, built-in weak pull-up resistor High level = read FIFO data, low level = read FIFO status
6	FULL	Output	FIFO full state output, active low
27	EMPT	Output	FIFO empty state output, active low
28	CLR	Input	Reset input, built-in weak pull-up resistor, active low
1, 3, 7, 8, 13, 14, 15, 17, 20, 22, 29, 32, 34, 43	NC.	NC	Connection disabled

5. Functional Specification

CH424 chip can be easily hooked to the system bus of various DSP and MCU through an 8-bit passive parallel interface, and can coexist with multiple peripheral devices. W_CS and R_CS chip selection pins of CH424 chip can be driven by the address decoding circuit, and can be used for device selection when MCU has multiple peripheral devices.

CH424 has two 8-bit passive parallel ports: input port W and output port R, and supports simultaneous operation on both ports.

On the input port W, the external MCU can query FIFO state through the 8-bit parallel interface at any time, and write the data into FIFO of CH424 when there is free space. The following table is the truth table of port W parallel operation.

W_CS	W_WR	W_RD	WD7～WD0	Actual operation on CH424
1	X	X	X/Z	CH424 is not selected and any operation is not performed
0	1	1	X/Z	Selected, but no operation
0	0	1	Input	Write data to FIFO
0	1	0	Output	Read the current FIFO free space and the number of bytes of free space
0	0	0	X/Z	Illegal state, forbidden to be used

On the output port R, the external MCU can query FIFO state through the 8-bit parallel interface at any time, and read the data in sequence when there is data in FIFO. The following table is the truth table of port R parallel operation.

R_CS	R_RD	R_A0	RD7～RD0	Actual operation on CH424
1	X	X	Z	CH424 is not selected and any operation is not performed
0	1	X	Z	Selected, but no operation
0	0	1	Output	Read data from FIFO
0	0	0	Output	Read the current FIFO used space and the number of bytes of stored data

FIFO is used to implement Port R-W data synchronization by asynchronous data buffer, for example, write piecemeal on port W, read in batch from port R, or write in batch on port W, read piecemeal on port R.

FIFO refers to the sequence that the data written first on the port W will be read firs on the port R, the data written later will be read later, the data read on the port R will be written from the port W.

FIFO memory capacity of CH424 is 4, 096 bytes, and the length range of data storage is 0000H ~ 1000H. Before reading and writing FIFO of CH424, the external MCU shall first query the state of FIFO, namely, the used space or the remaining space of FIFO.

On the port W, the current FIFO free space is queried; on the port R, the current FIFO used space is queried. They are collectively called the current FIFO available length (number of bytes).

The available length of FIFO is 13-bit binary number, and the external MCU needs to perform at least two read operations of FIFO state and combine them to get the current available length of FIFO. If the bit 7 (corresponding to the pin WD7 or RD7) of the returned data in “Read FIFO” state is 0, the bits 6-0 of the returned data will be the bits 6-0 of the available length of FIFO; if the bit 7 of the returned data in “Read FIFO” state is 1, the bit 5-0 of the returned data will be the bits 12-7 of the available length of FIFO; by combining the bits 12-0 of the two results, the available length of the current FIFO can be gotten.

CH424 chip incorporates a power on reset circuit and supports an external reset input from CLR pin to clear the FIFO count.

6. Parameters

6.1. Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter description		Min.	Max.	Unit
TA	Ambient temperature during operation	VCC=5V or VCC=3.3V	-40	85	℃
		VCC=3V	-20	70	℃

TS	Ambient temperature during storage	-55	125	℃
VCC	Supply voltage (VCC connects to power, GND to ground)	-0.5	6.0	V
VIO	Voltage on the input or output pins	-0.5	VCC+0.5	V

6.2. Electrical Parameters

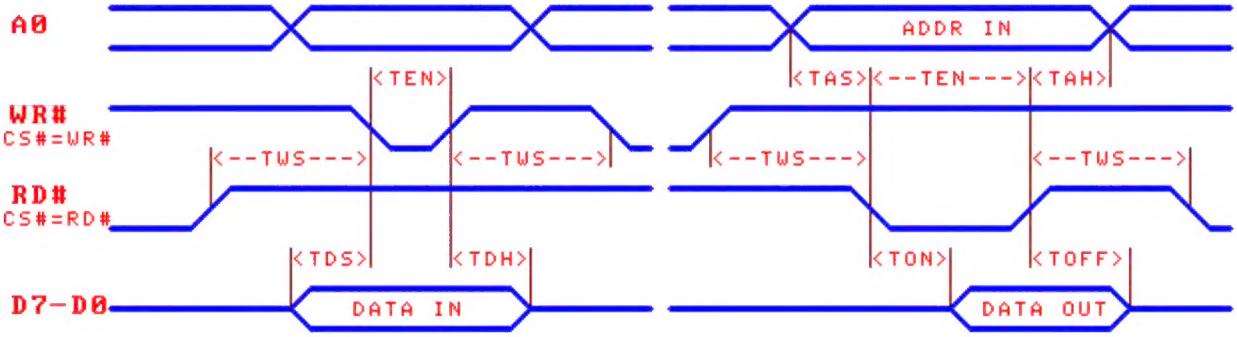
Test Conditions: TA=25℃, VCC=5V

Name	Parameter description	Min.	Typ.	Max.	Unit
VCC	Supply voltage	3.0	5	5.3	V
ICC	Static supply current	0.2	1	3	mA
VIL	Low level input voltage	-0.5		0.7	V
VIH	High level input voltage	2.0		VCC+0.5	V
VOL	Low level output voltage (4mA draw current)			0.5	V
VOH	High level output voltage (4mA output current)	VCC-0.5			V
IUP	Input current of input terminal for built-in weak pull-up resistor	1	5	20	uA
VR	Voltage threshold of power-on reset	2.4	2.7	3.0	V

6.3. Parallel Port Timing Parameters

Test Conditions: TA=25℃, VCC=5V, parameters in brackets apply to VCC=3.3V

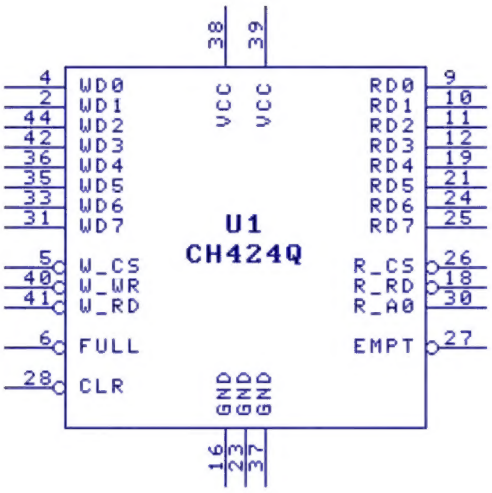
(WR# means that W_CS signal is valid and W_WR signal is valid; RD# means that R/W_CS signal is valid and R/W_RD signal is valid)



Name	Parameter description	Min.	Typ.	Max.	Unit
TEN	Pulse width of valid read strobe RD# or write strobe WR#	30 (40)			nS
TWS	Time interval between effective strobe pulse (recovery time)	50 (90)			nS
TAS	Address R_A0 setup time before the read strobe RD# is valid	0			nS
TAH	Address R_A0 hold time after the read strobe RD# is invalid	0			nS
TDS	Data WD0-WD7 setup time before the write strobe RD# is valid	0			nS

TDH	Data WD0-WD7 hold time after the write strobe WR# is invalid	0			nS
TON	Read strobe RD# valid until data output valid	2 (4)	18 (25)	25 (35)	nS
TOFF	Read strobe RD# invalid until data output invalid	2 (4)	22 (30)	30 (40)	nS

7. Applications

If there is no need to query the available length state of FIFO (port W is the free space and port R is the used space), there will be no need to connect W_RD pin on the port W and no need to connect R_A0 pin on the port R.

If there is no need to query the full and empty states of FIFO, there will be no need to connect the FULL and EMPT pins.